CLAIMS

What is claimed is:

1. A drive controller for a self-commutated converter having two half-bridges with converter valves, said drive controller comprising:

two control circuits, each control circuit being associated with a corresponding half-bridge and operatively connected with the converter valves of that half-bridge;

at least two switches, each switch having an input that is directly or indirectly connected to an external voltage and an output that is directly or indirectly connected to a pulse-inhibiting path;

at least two pulse-inhibiting controllers, each switch receiving control signals from a corresponding one of the pulse-inhibiting controllers; and

a buffer unit arranged in the pulse-inhibiting path for briefly maintaining a supply voltage of the control circuits if a pulse-inhibiting path electrically disconnects at least one of the control circuits from the external voltage.

2. The drive controller of claim 1, wherein the buffer unit includes a support capacitor having one input connected to ground and another input connected to a decoupling diode.

3. The drive controller of claim 1, wherein the buffer unit includes a support capacitor having one input connected to ground and another input connected to an output of a storage inductance, and a free-wheeling diode connected between an input of the storage inductance and ground.

4. The drive controller of claim 2, wherein a load resistor is connected electrically in parallel with the support capacitor.

5. The drive controller of claim 3, wherein a load resistor is connected electrically in parallel with the support capacitor.

6. The drive controller of claim 1, wherein the buffer unit has an input operating as a diagnostic terminal.

7. The drive controller of claim 1, wherein the at least two switches are electrically connected in series, with a first of the at least two switches being directly connected to the external voltage and a second of the at least two switches being directly connected to the pulse-inhibiting path.

8. The drive controller of claim 1, wherein the inputs of the at least two switches are directly connected to an external voltage and the output of each switch is directly connected to a different pulse-inhibiting path, with the different pulse-inhibiting paths disconnecting different control circuits.